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INPUT STAGE APPARATUS AND METHOD HAVING A VARIABLE REFERENCE VOLTAGE

TECHNICAL FIELD

The present invention relates generally to input stages generating an output signal having a predetermined logic level based on the voltage level of an input signal, and in particular, input stages having increased input signal noise margin.

BACKGROUND OF THE INVENTION

Integrated circuits typically include a number of input/output pins which are used for communication with additional circuitry. For example, an integrated memory device such as a dynamic random access memory (DRAM) includes both control inputs for receiving memory operation control signals, and data pins for bi-directional data communication with an external system or processor. Since the information provided to an integrated circuit through its pins include both control signals and data, it is important that the signals are accurately received and interpreted by the integrated circuit for proper operation.

In addition to the need to maintain the accuracy and integrity of signals provided to an integrated circuit, as integrated circuits have become smaller, and the demand for power efficient integrated circuits increases, the voltage levels of the input and output signals have continued to be reduced. Input and output signals having lower voltage swings have the benefit of lower switching times and lower power consumption. New circuitry and methods have been developed to accommodate the lower voltage levels while ensuring the accuracy and integrity of the data provided by the signals. For example, input stages generally provide an output signal having a defined logic level based on the voltage level of an input signal. Input stages have traditionally set the voltage levels at which the input signal causes either a logic HIGH or LOW output signal to be generated by designing input transistors having the appropriate sizes. However, to accommodate the reduced

voltage levels of the input signals, alternative methods and input stage designs have been developed.

One such input stage includes an input buffer that generates an output signal having a logic level based on the voltage level of an input signal relative to a reference voltage VREF. That is, where the input signal has a voltage level greater than the VREF voltage, the input buffer generates a HIGH output signal, and where the voltage level is less than the VREF voltage, a LOW output signal is generated. However, an issue with input signal noise margin may arise with these conventional input stages. As illustrated in Figure 1, where a constant reference voltage VREF is applied, it is possible to have inadvertent switching of an input buffer due to a noisy system bus. The reference voltage VREF is maintained at a steady voltage level VREFSSTL. When the IN signal crosses VREFSSTL due to noise, the input buffer switches the logic level of the output signal OUT. Thus, although the IN signal is intended to transition once from a relatively low voltage level to a relatively high voltage level at a time t_H, and then once again back to a relatively low voltage at a time t_L, the OUT signal switches logic levels a total of five times due to the noise of the IN signal.

Although system designers have attempted to reduce noise on system busses, and device designers have attempted to reduce susceptibility to input signal noise, the issue is nevertheless becoming more significant as the voltage levels of input signals continue to decrease. Therefore, there is a need for an input stage having improved input signal noise margin and having less susceptibility to inadvertent switching due to the input signal noise.

SUMMARY OF THE INVENTION

The present invention is directed to an input stage and method having increased input signal noise margin for generating an output signal having a predetermined logic level in response to receiving an input signal having a voltage level. The input stage includes an input buffer that includes an input to which the input signal is applied and an

output at which the output signal is provided. The input buffer also includes a reference terminal to which a reference voltage signal is applied. The input buffer generates an output signal having a logic level based on the voltage of the input signal relative to the voltage of the reference voltage signal applied to the reference terminal. The input stage further includes a voltage generator that generates a variable output voltage signal that is used as the reference voltage for the input buffer. The voltage of the output voltage signal provided by the voltage generator is dependent on the logic value of the output signal of the input buffer. In this manner, the reference voltage applied to the input buffer can be adjusted based on the logic level of the output signal in order to provide increased input signal noise margin.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a signal diagram illustrating various signals of a conventional input buffer.

Figure 2 is a signal diagram illustrating various signals of an input stage according to an embodiment of the present invention.

Figure 3 is a functional block diagram illustrating an input stage according to another embodiment of the present invention.

Figure 4 is a functional block diagram of an input stage according to an embodiment of the present invention.

Figures 5a and 5b are signal diagrams showing various signals of an input stage according to an embodiment of the present invention.

Figure 6 is a block diagram of a memory device including an input stage according to an embodiment of the present invention.

Figure 7 is a block diagram of a computer system including a memory device of Figure 6.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention are directed to an input stage having input buffer circuitry using a variable reference voltage to improve input signal noise margin. Certain details are set forth below to provide a sufficient understanding of the invention. However, it will be clear to one skilled in the art that the invention may be practiced without these particular details. In other instances, well-known circuits, control signals, and timing protocols have not been shown in detail in order to avoid unnecessarily obscuring the invention.

Figure 2 is a signal diagram illustrating various signals of an input stage according to embodiments of the present invention. It will be appreciated that Figure 2 is not drawn to scale. As with Figure 1, which illustrated various signals of the prior art input buffer circuitry, Figure 2 illustrates an input signal IN to the input stage, an output signal OUT provided by the input stage in response to the IN signal, and a reference voltage VREF. However, in contrast to Figure 1, the VREF voltage illustrated in Figure 2 is variable. That is, the VREF voltage changes in accordance with the logic level of the OUT signal. The VREFSSTL voltage is also shown in Figure 2 for the purposes of comparison. As shown in Figure 2, two different voltage levels are used for VREF, a high reference voltage VREFH, which is used for determining when to generate an OUT signal having a HIGH logic level in response to a HIGH IN signal, and a low reference voltage VREFL, which is used for determining when to generate an OUT signal having a LOW logic level in response to a LOW IN signal. In contrast to Figure 1, the OUT signal illustrated in Figure 2 does not fluctuate in response to the noise of the IN signal because of the increased noise margin provided by the use of a variable reference voltage.

Figure 3 illustrates a series-stub-terminated logic (SSTL) input stage 300 according to embodiments of the present invention. A constant reference voltage VREFSSTL is applied to a non-inverting input of an operational amplifier 302, as known in the art. A resistive voltage divider circuit 306, which includes resistors 308a-308d, is coupled to the output of the op-amp 302. The voltage at a node between the second and

third resistors 308b and 308c, respectively, is provided back to the inverting input of the op-amp 302. As a result, the op-am 302 will generate an output signal having a voltage such that the voltage provided back to the inverting input is approximately equal to VREFSSTL. Consequently, the voltage at the output of the op-amp 302 is greater than the VREFSSTL voltage. As shown in Figure 3, a high reference voltage VREFH is generated at a node 310 located between the first and second resistors 308a and 308b, respectively, and is provided to a multiplexer 314. A low reference voltage VREFL is also generated at a node 312 located between the third and fourth resistors 308c and 308d, respectively, and is provided to a multiplexer 316. Both multiplexers 314 and 316 can be of conventional design known in the art. As mentioned previously, the VREFH voltage is relatively higher than the VREFSSTL voltage, and the VREFL voltage is relatively lower than the VREFSSTL voltage. It will be appreciated that the VREFH and VREFL voltages can be adjusted relative to one another by changing the relative resistance values of the resistors 308a-308d. In an embodiment of the input stage 300, one or more of the resistors 308a-308d consists of a variable resistor, as well known in the art, to allow for the VREFH and VREFL voltages to be adjusted.

The VREFSSTL voltage is also applied to a terminal of a capacitor 320a that is coupled to the node 310 and a terminal of a capacitor 320b that is coupled to the node 312 in order to respond to fluctuations in the VREFSSTL voltage. That is, by coupling the VREFSSTL voltage to nodes 310 and 312 through capacitors 320a and 320b, respectively, the voltage at the respective nodes will maintain the relative relationship with the VREFSSTL voltage. Thus, the voltages of VREFH and VREFL with respect to the VREFSSTL voltage will be held relatively constant. The capacitors 320a and 320b additionally smooth fluctuations in the VREFH and VREFL voltages.

The multiplexer 314 provides the VREFH voltage to a VREF input of an SSTL input buffer 330 in response to an active selection signal SELECT VREFH. Similarly, the multiplexer 316 provides the VREFL voltage to the VREF input of the SSTL input buffer 330 in response to an active selection signal SELECT VREFL. An external

input signal XQS is applied to an IN input of the input buffer 330. The input buffer 330, which can be of a conventional design known in the art, compares the voltage of the input signal to the reference voltage applied to the VREF input, and generates an output signal having an appropriate logic level at an output terminal. The output value QS generated by the input buffer 330 is also provided to a selection circuit 334 for generating the SELECT VREFH and SELECT VREFL signals for the multiplexers 314 and 316. As will be explained in more detail below, the selection circuit 334 provides an active selection signal to the appropriate multiplexer in response to the logic level of the QS signal. Consequently, the reference voltage applied to the VREF input to the input buffer 330 will be selected based on the logic level of the output signal.

As will be explained in greater detail below, embodiments of the present invention use a variable voltage as the reference voltage for the input buffer 330, the voltage of which is a function of the logic state of the input buffer. More specifically, if the output signal of the input buffer 330 has a HIGH logic level, then a reference voltage having the VREFL voltage, where VREFL < VREFSSTL, is provided to the input buffer 330 as VREF. Where the output signal of the input buffer 330 is a LOW logic level, then a reference voltage having the VREFH voltage, where VREFH > VREFSSTL, is provided to the input buffer 330 as VREF. With this arrangement, the input stage will not switch as soon as the input crosses VREFSSTL. Once the input stage generates a HIGH logic level, the reference voltage switches, and the voltage of the input signal will need to be lower than VREFL for a LOW output signal to be generated. Once the input stage generates a LOW logic level, the reference voltage switches, and the voltage of the input signal will need to be greater than VREFH for a HIGH output signal to be generated. In effect, input stages according to embodiments of the present invention have a built in hysteresis by using a variable VREF, consequently, resulting in improved noise immunity.

Figure 4 is a schematic drawing of a portion of the input stage 300 illustrated in Figure 3. Operational amplifier block 402 represents the op-amp 302 and the voltage divider circuit 306 (Figure 3). Transfer gates 414 and 416 represent the

multiplexers 314 and 316, respectively. As illustrated in Figure 4, coupled to the output of the input buffer 330 are a transfer gate 404 and a pair of inverters 406 and 410. The control terminals of the transfer gate 404 are tied to a respective reference voltage to couple the output of the input buffer 330 to the input of an inverter 406. The output of the inverter 406 and an inverter 412 are provided to control terminals of the transfer gates 414 and 416 to select between the VREFH and VREFL as the VREF input of the input buffer 330. Specifically, where the output signal of the input buffer 330 has a HIGH logic level, the transfer gate 416 is activated to couple the node 312 to the VREF input to provide the VREFL voltage as the reference voltage, and where the output signal of the input buffer 330 has a LOW logic level, the transfer gate 414 is activated to couple the node 310 to the VREF input to provide the VREFH voltage.

Operation of the input stage 300 will be described with respect to Figures 5a and 5b. Figure 5a illustrates the output signal QS in response to an input signal XQS. The signal applied to the VREF input of the input buffer 330 (Figure 3) is represented by the signal VREFVAR. For the purposes of comparison, Figure 5a also illustrates the output signal QS_REF generated by an input buffer having a constant reference voltage applied to its VREF input. The constant reference voltage is represented in Figure 5a as VREFSSTL.

At a time t_0, the XQS signal makes a transition from a relatively low voltage level to a relatively high voltage level. With respect to the receiving a constant VREFSSTL reference signal, at a time t_1 the XQS signal exceeds the VREFSSTL voltage level, and as a result, the output signal QS_REF switches to a HIGH logic level at a time t_3. For the input buffer 330 having the VREFVAR signal applied to its VREF input, the XQS signal exceeds the VREFVAR signal at a time t_2, which in turn causes the input buffer 330 to output a HIGH QS signal at a time t_4. As previously discussed, in response to the QS signal going HIGH, the VREFVAR signal falls to a VREFL voltage level shortly after time t_4 in order to provide improves noise margin with respect to the XQS signal.

At a time t_5, the XQS signal makes a transition from a relatively high voltage level to a relatively low voltage level. The voltage of the XQS signal falls below

the VREFSSTL voltage level at a time t_6, and in response the QS_REF signal switches from a HIGH logic level to a LOW logic level at a time t_8. At a time t_7, the voltage of the XQS signal falls below the VREFL voltage, causing the input buffer 330 to force the QS signal from HIGH to LOW at a time t_9. In response to the transition in the QS signal, the VREFVAR signal switches from the VREFL voltage to a VREFH voltage to provide increased noise margin for the XQS signal.

As illustrated by Figure 5a, the input buffer 330 which receives a variable reference voltage applied to its VREF input produces the same output as the conventional input buffer using a constant reference voltage, but provides improved noise margin for the input signal XQS. The noise margin for the input buffer with a variable reference voltage is represented in Figure 5a as $N_{mH,VREFVAR}$ and $N_{mL,VREFVAR}$. Compared with the noise margin for the input buffer with the constant reference voltage, that is, $N_{mH,VREFSSTL}$ and $N_{mL,VREFSSTL}$, the noise margins of $N_{mH,VREFVAR}$ and $N_{mL,VREFVAR}$ are clearly greater. It will appreciated that although the difference in the voltage values of VREFL and VREFH relative to the VREFSSTL signal are illustrated in Figure 5a as being approximately equal, the voltages of VREFL and VREFH may be tailored, as previously described, such that the differences are unequal if so desired. That is, the VREFL and VREFH voltage levels can be controlled independently to meet specific design requirements.

A time delay Δt_r and Δt_f between the output signals of the input buffer receiving the constant reference voltage VREFVAR, and the input buffer stage receiving the variable reference voltage VREFSSTL. The time delays Δt_r and Δt_f result from the difference in the reference voltage applied to an input buffer. That is, it takes more time for an input signal to exceed the threshold for the variable reference voltage, either VREFL or VREFH, than for the constant reference voltage VREFSSTL. The time delay will be affected by the slew rate of the input signal XQS. It will be appreciated that the time delays are minimal and the additional noise margin afforded by the variable reference voltage is a benefit that may outweigh any adverse affect on device performance.

Figure 5b illustrates the advantage provided by embodiments of the present invention over conventional input stages. In Figure 5b, the input signal XQS simulates a "noisy" input signal. That is, at a time t_0, the XQS signal makes a transition from a relatively low voltage level to a relatively high voltage level. Input signal noise is simulated by decreasing the voltage of the XQS signal ΔV_H at a time t_2. The voltage level is maintained until a time t_5, at which time the XQS signal makes a transition to a relatively low voltage level. At a time t_8, input signal noise is simulated by increasing the voltage of the XQS signal ΔV_L. The noise level is maintained until a time t_{11}, where the XQS signal makes a transition back to a relatively high voltage level.

With respect to the output signals, QS_REF represents the output signal of an input buffer receiving a constant reference voltage VREFSSTL, and QS represents the output signal of an input buffer receiving a variable reference voltage VREF. Approximately at a time t_1, QS_REF and QS make a transition to a HIGH logic level in response to the XQS signal exceeding the voltages VREFSSTL and VREF, respectively. The transition to the HIGH logic level of the QS signal causes the VREFVAR signal to change to a VREFL voltage, which as a result, increases input signal noise margin. As mentioned previously, input signal noise is simulated at a time t_2 by decreasing the voltage of the XQS signal ΔV_H. The change in the voltage ΔV_H results in the XQS signal dropping below the VREFSSTL voltage at a time t_3. In response, the QS_REF signal makes a transition to a LOW logic level at a time t_4, although the change in voltage ΔV_H merely represents input signal noise. In contrast, because the variable reference voltage VREFVAR is set to the VREFL voltage, providing increased noise margin, the QS signal is unaffected by the introduction of noise to the XQS signal at a time t_2. The QS signal does not transition to a LOW logic level until a time t_7, which is in response to switching to a relatively low voltage level at time t_5 and the voltage of the XQS signal exceeding the VREFL voltage at a time t_6. As illustrated by the present example, the use of a variable reference voltage VREFVAR as the reference voltage for an input buffer can provide

additional input noise margin that reduces susceptibility to inadvertent switching due to input signal noise.

Following the transition of the QS signal at time t_7 from a HIGH logic level to a LOW logic level, the VREFVAR voltage is adjusted to the VREFH voltage to provide additional noise margin for the XQS signal. As previously described, at a time t_8, the voltage of the XQS is increased by a ΔV_L voltage to simulate input signal noise, although the change in voltage ΔV_L merely represents input signal noise. The resulting XQS signal exceeds the constant reference voltage VREFSSTL at a time t_9, and consequently, the QS_REF signal makes a transition from a LOW logic level to a HIGH logic level at a time t_{10}. The QS signal, on the other hand, remains at the LOW logic level despite the input noise ΔV_L, and does not make a transition to a HIGH logic level until a time t_{13}, which is in response to the XQS signal making a transition at a time t_{11} and having a voltage exceeding the VREFH voltage at a time t_{12}. As with the previous example where noise was simulated for an input signal having a HIGH logic level, the QS signal was resistant to fluctuations for a LOW XQS signal having a noise of ΔV_L.

The present example more clearly demonstrates the advantages provided by using a variable reference voltage as the reference voltage for an input driver in order to provide increased input noise margin.

Figure 6 is a block diagram of a dynamic random access memory ("DRAM") 600 that includes an address decoder 602, control circuit 604, and read/write circuitry 606. The address decoder 602, control circuit 604, and read/write circuitry 606 are all coupled to a memory-cell array 608. In addition, the address decoder 602 is coupled to an address bus, the control circuit 604 is coupled to a control bus, and the read/write circuit 606 is coupled to a data bus. In operation, external circuitry, such as a processor or memory controller, applies address, data, and control signals on the respective busses to transfer data to and from the DRAM 600. As illustrated in Figure 6, input stages 620 according to embodiments of the present invention are included in the address decoder 602, the control circuit 604, and the read/write circuitry 606. The input stages 620 receive input

signals and, based on the voltage levels of the input signals, generate output signals having the appropriate logic levels for the respective circuitry. It will be appreciated that although Figure 6 shows an input stage 620 included in the address decoder 602, the control circuit 604, and the read/write circuitry 606, the input stage 620 can be included in greater or fewer of the functional circuit blocks without deviating from the scope of the present invention. Moreover, the input stage 620 could also be included in other memory cell circuit blocks that are well known, where inclusion of an input stage is appropriate.

Figure 7 is a block diagram of a computer system 700 including computing circuitry 702. The computing circuitry 702 contains a memory 701 that includes input stage circuitry according to embodiments of the present invention. The computing circuitry 702 performs various computing functions, such as executing specific software to perform specific calculations or tasks. In addition, the computer system 700 includes one or more input devices 704, such as a keyboard or a mouse, coupled to the computer circuitry 702 to allow an operator to interface with the computer system. Typically, the computer system 700 also includes one or more output devices 706 coupled to the computer circuitry 702, such output devices typically being a printer or a video terminal. One or more data storage devices 708 are also typically coupled to the computer circuitry 702 to store data or retrieve data from external storage media (not shown). Examples of typical storage devices 708 include hard and floppy disks, tape cassettes, and compact disc read-only memories (CD-ROMs). The computer circuitry 702 is typically coupled to the memory device 701 through appropriate address, data, and control busses to provide for writing data to and reading data from the memory device.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.